The opinion in support of the decision being entered today and is *not* binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte GUY L. STEELE JR.

Appeal 2007-3623
Application 10/035,747
Technology Center 2100

Decided: October 10, 2007

Before: HOWARD B. BLANKENSHIP, ALLEN R. MACDONALD, and ST. JOHN COURTENAY III, *Administrative Patent Judges*.

MACDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 from a Final Rejection of claims 1-54. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant invented systems and methods for performing floating point arithmetic computations, and more particularly systems and methods for performing floating point computations which use an enhanced format for the floating point operand. (Spec. [001]).

Representative independent claims 1 and 33 under appeal read as follows:

1. A floating point operand data structure used in floating point computations and processing within a processing device, comprising:

a first portion of the data structure having floating point operand data; and

a second portion of the data structure having embedded status information associated with at least one status condition of the floating point operand data.

33. A method of encoding a floating point operand with status information without maintaining the status information in a floating point status register, comprising:

determining a status condition of the floating point operand as part of processing the floating point operand in association with a floating point operation; and

representing an updated status condition of the floating point operand within the floating point operand.

The Examiner separately rejected claims 1-54 under 35 U.S.C. § 102(b) based on two patents.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Huang	US 5,995,991	Nov. 30, 1999
Lynch	US 6,009,511	Dec. 28, 1999

Appellant contends that the claimed subject matter is not disclosed in the prior art. More specifically, Appellant contends Huang fails to disclose status information within the floating point operand as required by claims 1-54 because the tag of Huang is separate from the operand. (Br. 13-23 and Reply Br. 5-9). Additionally, Appellant contends the Examiner fails to address how Huang discloses the feature of "a control unit . . . receiving at least one floating point instruction" as required by claims 21-26, 31, and 32. (Br. 17 and Reply Br. 9).

The Examiner contends that in Huang the tag is part of the floating point operand. (Answer 26-29).

Further, Appellant contends Lynch fails to disclose status information within the floating point operand as required by claims 1-54 because the tag of Lynch is separate from the operand. (Br. 23-34 and Reply Br. 9-13).

The Examiner contends that in Lynch the tag is part of the floating point operand. (Answer 29-32).

We affirm-in-part.

ISSUE(S)

Has Appellant shown that the Examiner has failed to establish Huang describes "status information within the floating point operand" as required by claims 1-54?

Has Appellant shown that the Examiner has failed to establish Huang describes the "control unit . . ." required by claims 21-26 and 31-32?

Has Appellant shown that the Examiner has failed to establish Lynch describes "status information within the floating point operand" as required by claims 1-54?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Huang

1. The prior art Huang patent describes that "[i]f the generation of the result produces one of a predetermined set of special operands, a tag generator also generates a tag having a predetermined tag value corresponding to the produced special operand." (Col. 5, ll. 43-46).

2. The prior art Huang patent describes that "each of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2." (Col. 6, l. 66 through col. 7, l. 2).

3. Figures 1-3 of Huang show a conventional arithmetic calculation circuit where one or more operands x and y are supplied from a memory device, such as a register file 12 and the operands x and y are inputted to an arithmetic section 14. (Col. 1, ll. 40-42).

4. In the conventional circuit, a zero value result (+ or -) is represented by an operand where (col. 1, ll. 56-64):

sign= '0' or '1' bit,

exponent=a sequence of eight '0' bits,

magnitude=a sequence of twenty-three '0' bits.

5. In the conventional circuit, when the arithmetic section 14 performs an operation that results in a value other than an ordinary operand value, the arithmetic unit outputs a signal indicating that the result is zero, infinity or not a number to the generator circuit 22. In response, the circuit 22 generates the appropriate output floating point number as per the IEEE standard of special operands set. (Col. 2, ll. 55-59).

6. In the conventional circuit, interposed between the register file and the arithmetic section 14 are detectors 24 and 26. One detector 24 or 26 is provided for each operand input path. The detectors 24 and 26 each receive a respective operand x or y and determines whether or not the received operand represents a special operand. If not, the detector 24 or 26 simply outputs the operand x or y to the arithmetic section 14. However, if the detector 24 or 26 detects that the operand x or y represents a special operand, the detector 24 or 26 identifies the type of the operand--the detector determines which of the special operands the received operand x or y represents. (Col. 3, ll. 11-21).

7. FIG. 2 shows an exemplary special operand generator circuit 22 in greater detail. As shown, the special operand generator circuit 22 includes first and second multiplexers 222 and 224.

8. In the conventional circuit, the arithmetic section 14 outputs appropriate selector control signals to the multiplexer 222 to output a resulting exponent, and to the multiplexer 224 to output a resulting magnitude of an arithmetic operation. (Col. 3, ll. 42-45 and 60-63).

9. In the conventional circuit, when the result of an arithmetic operation is zero, the arithmetic section outputs selector control signals to the multiplexers 222 and 224 for selecting the eight '0' bits for the exponent and twenty-three '0' bits for the magnitude. (Col. 3, ll. 66-67 through col. 4, ll. 1-4).

10. FIG. 3 shows a conventional detector 24 or 26. As shown, the detector 24 or 26 includes two comparator circuits 252 and 254. (Col. 4, ll. 24-26).

11. In the conventional circuit, three AND gates 261, 262 and 263 are also provided. The AND gate 261 receives as inputs the logic bits outputted on the lines 255 and 257. The AND gate 261 therefore outputs a signal indicating whether or not the operand represents a zero valued special operand. (Col. 4, ll. 41-45).

12. The prior art Lynch patent describes that the "FPU [floating point unit] core uses the tag value associated with an operand to determine whether the operand is a special floating point number." (Col. 16, ll. 62-65).

PRINCIPLES OF LAW

On appeal, Appellant bears the burden of showing that the Examiner has not established a legally sufficient basis for anticipation based on the Huang patent.

Appellant may sustain this burden by showing that the prior art reference relied upon by the Examiner fails to disclose an element of the claim. It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

ANALYSIS

Claim Interpretation

Claims 1-20 recite a "floating point operand data structure" and require status information be embedded within the data structure.

As to dependent claims 2-15 and 17-20, these claims fail to recite further structural or functional limitations of the data structure of claims 1 or 16. Rather, each of these dependent claims merely indicate the origin or intended use of the information in the data structure, indicate the numerical value of the operand, or indicate what the data within the operand will represent. Such claims do not further limit the data structure itself.

Claims 21- 54 require status information within a floating point operand. However, unlike claims 1-20, the language of claims 21-54 does not preclude the result (data) and the status information from being represented by the same bits within a floating point operand. See FF 4 above for an example of a floating point operand whose bits result in a value

of "zero" and whose bit string has been assigned a status of representing "zero."[1]

Additionally, claims 21-26, 31, and 32 require a control unit for handling a "floating point instruction," and claims 40-43 and 51-54 require "receiving a floating point instruction."

Finally, claims 28, 35, 37, 46, and 48 fail to further limit the claimed structure or functions. Rather, these claims merely recite the content of the status information and do not further limit the claims from which they depend.

Huang

As to claims 1-20, Appellant correctly points out that Huang does not describe the invention of claims 1-20. Appellant has established that the Examiner erred with respect to this contention as to claims 1-20.

As to claims 21-54, Appellant correctly points out that the device of figure 4 of Huang relied on by the Examiner does not describe status information embedded within a floating point operand as required by claims 21-54. Contrary to the Examiner's contention (Answer 27), Huang's "tag value" does not constitute a teaching data within the floating point operand as claimed. Rather, Huang discloses that the tag (status info) stands separate from the operand (result). (FF 1 and 2).

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[1] We note that these claims would distinguish over the cited prior art based on the operand if the claims were amended to require a single resulting floating point operand that contains distinct parts which represent a value and encoded status information.

However, Prior Art figures 1-3 of Huang teach all the features of claims 27-30, 33-39 and 44-50. See FF 3-11. Claims 27, 29, and 30 are exemplary. Claim 27 – an operand memory register (item 12) and a functional processing unit (items 14, 22, 24 & 26). Claim 29 – at least one predetermined field (See FF 4). Claim 30 – without storing status information separately (inherent).

For the special case of addition of the "zero" operand plus the "zero" operand to yield the "zero" operand, the conventional circuit corresponds to the subject matter of Appellant's claims 27-30, 33-39, and 44-50. Thus, contrary to Appellant's ultimate contention, Huang does disclose the subject matter of claims 27-30, 33-39, and 44-50.

Therefore, Appellant has not established that the Examiner erred with respect to this contention as to claims 27-30, 33-39, and 44-50. However, because figures 1-3 of Huang fail to describe a "floating point instruction," Appellant has established that the Examiner erred with respect to this contention as to claims 21-26, 31, 32, 40-43, and 51-54.

Lynch

The Lynch patent parallels the Huang patent in that both append a status tag to a floating point operand to improve on the conventional method of handling special status operands. As above with Huang, Appellant correctly points out that the appended tags of Lynch do not correspond with the limitations of claims 1-54.

Appellant has established that the Examiner erred with respect to the rejection of claims 1-54.

NEW GROUNDS OF REJECTION

35 U.S.C. § 102

Our decision relies on different reasoning with respect to the Huang patent than that set forth by the Examiner. Due to our new reasoning, we designate our decision as a new ground of rejection.

35 U.S.C. § 101

We reject claims 1-20 under 35 U.S.C. § 101, using our authority under 37 C.F.R. § 41.50(b).

Claims 1-20 are directed to a data structure per se and as such these claims are directed to non-statutory subject matter. Appellant should compare his claims 1-20 to the statutory "memory containing a stored data structure" found in *Lowry*, 32 F.3d 1579, 32 USPQ2d 1031(Fed. Cir. 1994).

35 U.S.C. § 112, second paragraph

We reject claims 31-32 under 35 U.S.C. § 112, second paragraph, using our authority under 37 C.F.R. § 41.50(b).

Claims 31 and 32 are indefinite because "the floating point instruction" of claim 31 lacks an antecedent basis.

37 C.F.R. § 41.50(b)

37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of appeal as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ...
>
> (2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record ...

OTHER ISSUES

The Board of Patent Appeals and Interferences is a review body, rather than a place of initial examination. We have made a rejection above under 37 C.F.R. § 41.50(b). However, we have not reviewed claims 21-26, 40-43, and 51-54 to the extent necessary to determine whether these claims are patentable over the Huang patent in combination with Appellant's prior art admissions (see Appellant's figures 1-2 and related specification). We leave it to the instant Examiner to determine the appropriateness of any further rejections based on these references.

CONCLUSION OF LAW

(1) Appellant has not established that the Examiner erred in rejecting claims 27-30, 33-39 and 44-50 as being unpatentable under 35 U.S.C. § 102(b) over Huang.

(2) Appellant has established that the Examiner erred in rejecting claims 1-26, 31, 32, 40-43, and 51-54 as being unpatentable under 35 U.S.C. § 102(b) over Huang.

(3) Appellant has established that the Examiner erred in rejecting claims 1-54 as being unpatentable under 35 U.S.C. § 102(b) over Lynch.

(4) Claims 1-20, 27-39, and 44-50 are not patentable.

(5) On this record, claims 21-26, 40-43, and 51-54 have not been shown to be unpatentable.

DECISION

The Examiner's rejection of claims 27-30, 33-39 and 44-50 is Affirmed.

The Examiner's rejection of claims 1-26, 31, 32, 40-43, and 51-54 is Reversed.

We reject claims 1-20 under 35 U.S.C. § 101.

We reject claims 31-32 under 35 U.S.C. § 112, second paragraph.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART
37 C.F.R. § 41.50(b)

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SUN MICROSYSTEMS/FINNEGAN, HENDERSON LLP
901 NEW YORK AVENUE, NW
WASHINGTON DC 20001-4413